

FIG. 1A
(PRIOR ART)

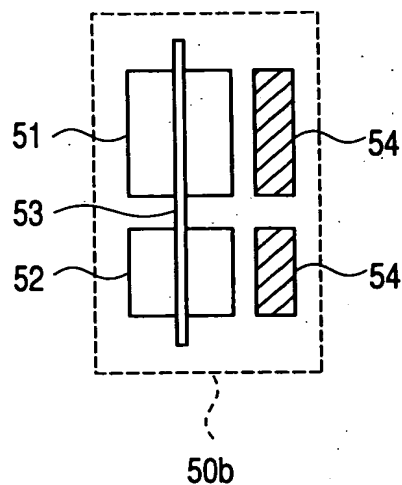


FIG. 1B
(PRIOR ART)

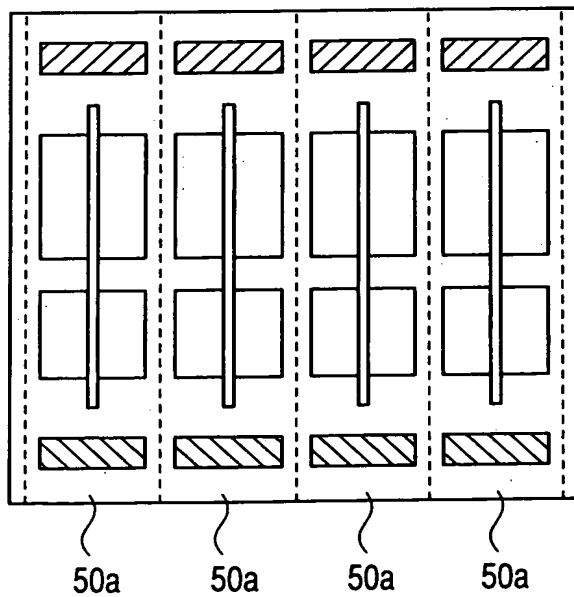


FIG. 2
(PRIOR ART)

FIG. 3B

Figure 1 is a plan view of a semiconductor device. The device is divided into two main regions: 2 (N-well) and 3 (P-well). The top portion of the device shows a first array of memory cells (10) with word lines (14) and bit lines (15). A second array (16) is shown with a different bit line configuration. The bottom portion shows a second array of memory cells (10) with word lines (14) and bit lines (15). A third array (16) is shown with a different bit line configuration. The device is divided into regions 2 (N-well) and 3 (P-well).

FIG. 4B

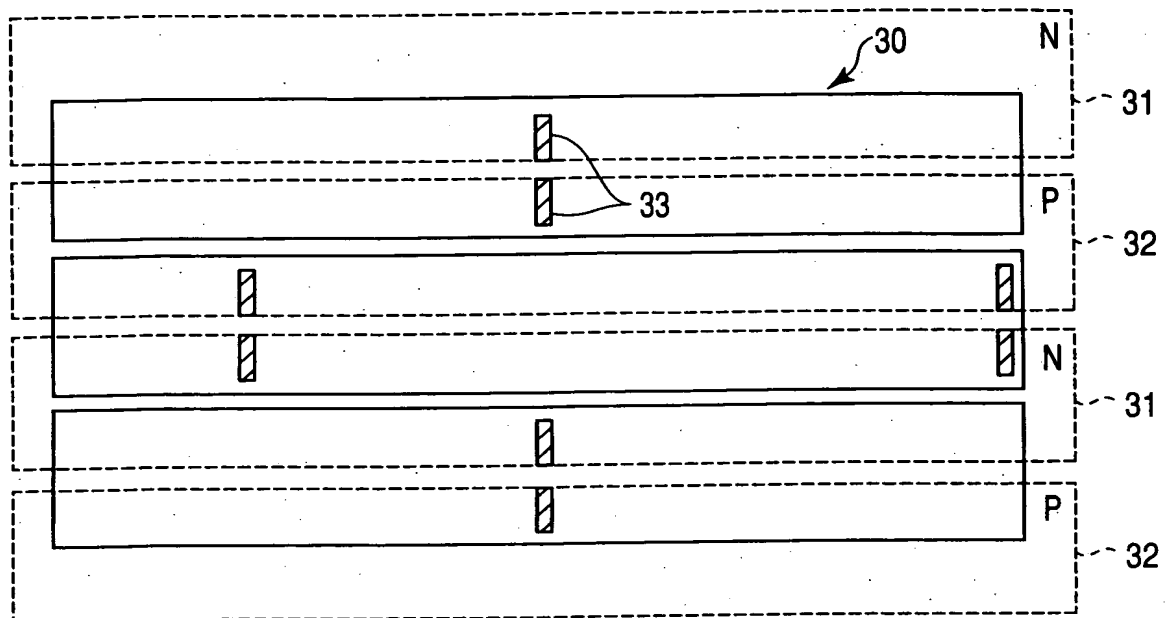


FIG. 5A

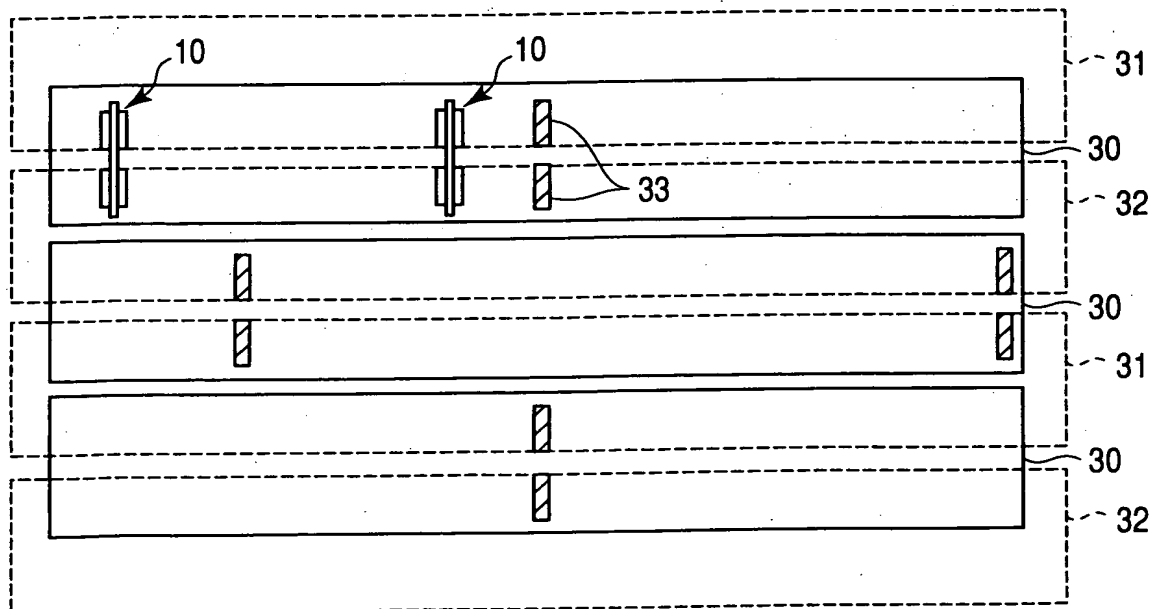


FIG. 5B

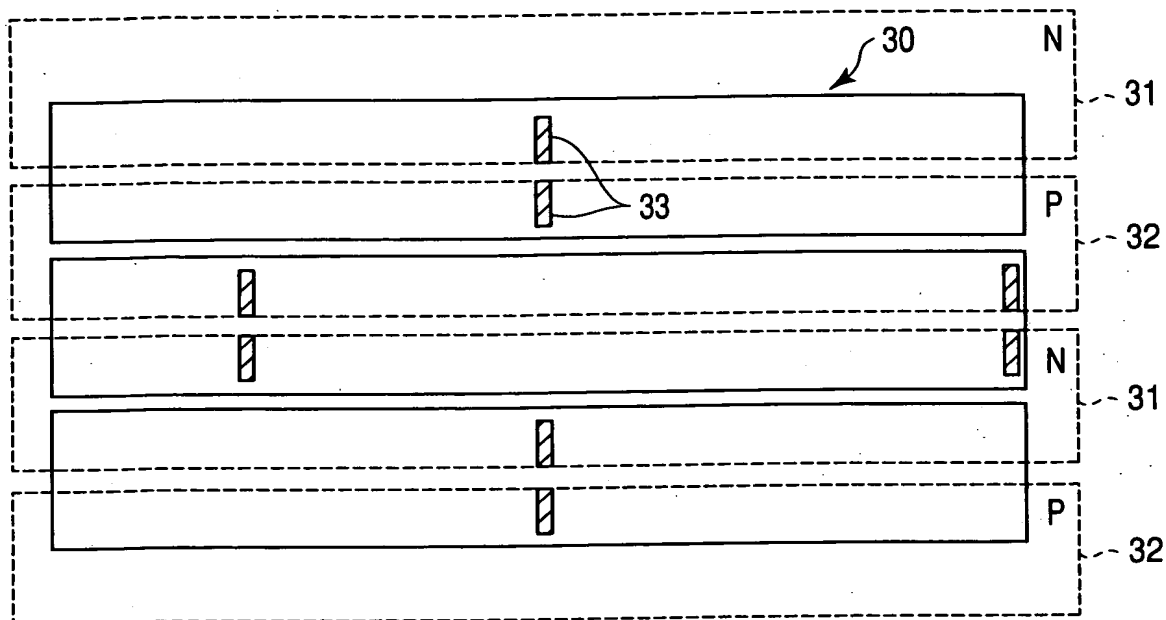


FIG. 6A

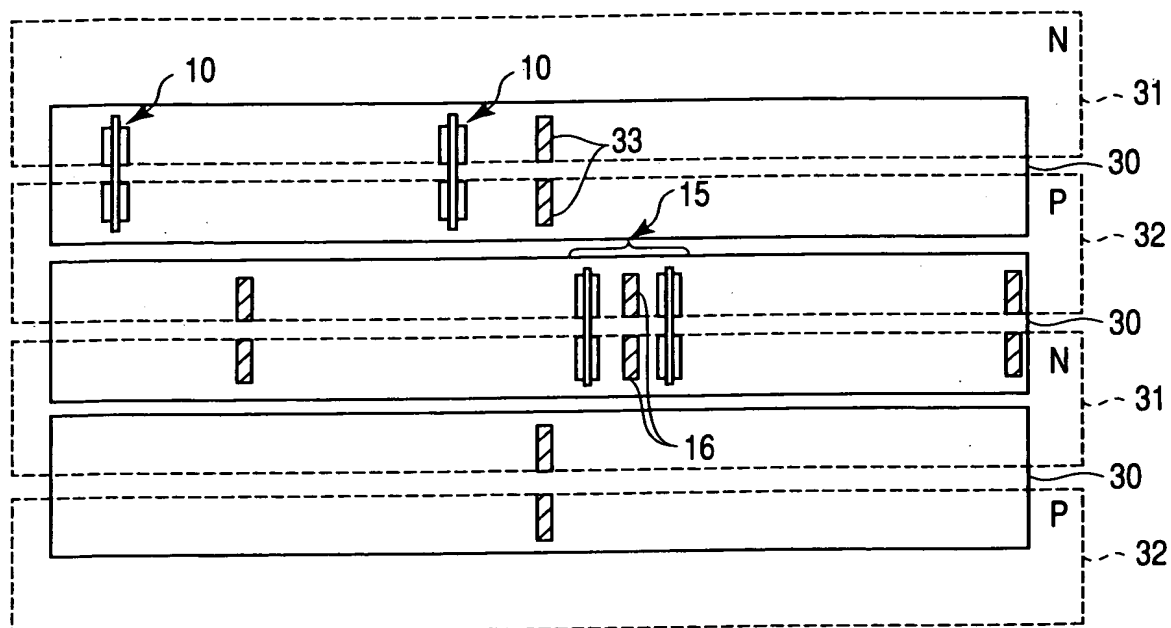


FIG. 6B